

Jabalpur Engineering College, Jabalpur
Semester VI Credit Based Grading System (CBGS) w.e.f. July 2017
 Scheme of Examination

Bachelor of Engineering B.E. (Electronics & Telecommunication Engineering)
Subject wise distribution of marks and corresponding credits
Scheme of Examination w.e.f. July-2017 (Academic Session-2017-18)

S. No.	Subject Code	Subject Name & Title	Maximum Marks Allotted						Hours / week.			Total Credits	Total Marks
			Theory			Practical		Total Marks					
			End Sem	Mid Sem. MST	Quiz, Assignment	End Sem.	Lab Work		L	T	P		
1	EC6001	Antenna & Wave Propagation	70	20	10	-	-	100	3	1	-	4	
2	EC6002	Microprocessor & Microcontroller	70	20	10	30	20	150	3	1	2	6	
3	EC6003	CMOS VLSI	70	20	10	30	20	150	3	1	2	6	
4	EC6004	Digital Signal Processing	70	20	10	30	20	150	3	1	2	6	
5	EC6005	Elective-II	70	20	10	-	-	100	3	1	-	4	
6	EC6006	Departmental Lab-III (Departmental Choice) VHDL/Verilog	-	-	-	30	20	50	-	-	2	2	
7	EC6007	Creativity and Entrepreneurship Development (Internal Assessment)	-	-	-	-	50	50	-	-	2	2	
8	EC6008	Startup / Industrial Lectures (Internal Assessment)	-	-	-	-	50	50	-	-	2	2	
Total			350	100	50	120	180	800	15	5	12	32	800

MST: Minimum of two mid semester tests to be conducted.

- Students have to go for Industrial Training /Internship of 4 weeks at the end of VI Semester.

L: Lecture

T: Tutorial

P: Practical

Department Elective-II (Four Subjects)	
Subject Code	Subject Name
EC6005A	IPR (Intellectual Property Right)
EC6005B	Data Communication & Computer Network
EC6005C	Power Electronics
EC6005D	Operating System

[Signature]

Dr. SHAILJA KUMAR
 Head of Department
 Jabalpur Engineering College
 Jabalpur - 482 011 (M.P.)

B.E. (CBGS) VI SEMESTER

ELECTRONICS & TELECOMMUNICATION ENGINEERING

ANTENNA AND WAVE PROPAGATION

Course	Subject Title	Subject Code	Grade for End Sem.		CGPA at the end of every even semester
			T	P	
B.E. (CBGS)	Antenna and Wave Propagation	EC6001	Min. "D"	Min. "D"	5.0

Unit -I:

Introduction to antenna: Antenna terminology, radiation, retarded potential, radiation field from current element, radiation resistance of short dipole and half wave dipole antenna, network theorems applied to antenna, self and mutual impedance of antenna, effect of earth on vertical pattern and image antenna.

Unit -II:

Antenna arrays: of point sources, two element array, end fire and broad side arrays, uniform linear arrays of n-elements, linear arrays with non-uniform amplitude distribution (binomial distribution and Chebyshev optimum distribution), arrays of two-driven half wavelength elements (broad side and end fire case), principle of pattern multiplication.

Unit -III:

Types of antennas: Babine's principles and complementary antenna, horn antenna, parabolic reflector antenna, slot antenna, log periodic antenna, loop antenna, helical antenna, biconical antenna, folded dipole antenna, Yagi-Uda antenna, lens antenna, turnstile antenna. Long wire antenna: resonant and travelling wave antennas for different wave lengths, V-antenna, rhombic antenna, beverage antenna, micro strip antenna.

Unit -IV:

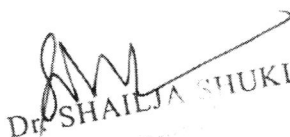
Antenna array synthesis: introduction, continuous sources, methods-Schelkn off polynomial method, Fourier transform method, Woodward- Lawson method, Taylor's method, Laplace transform method, Dolph- Chebychev method, triangular, cosine and cosine squared amplitude distribution, line source, phase distribution, continuous aperture sources.

Unit -V:

Propagation of radio wave: Structure of troposphere, stratosphere and ionosphere, modes of propagation, ground wave propagation, duct propagation. Sky wave propagation: Mechanism of Radio Wave Bending by Ionosphere, critical angle and critical frequency, virtual height, skip distance and LUF, MUF. Single hop and multiple hop transmission, influence of earth's magnetic field on radio wave propagation, Fading Space Wave Propagation: LOS, effective earth's radius, field strength of space or tropospheric propagation.

Books References:

1. J. D. Krauss: Antennas;for all applications, TMH.
2. R. E. Collin, Antennas and Wave Propagation, Wiley India Pvt. Ltd.
3. C. A. Balanis: Antenna Theory Analysis and Design, Wiley India Pvt. Ltd.
4. Jordan and Balmain: Electromagnetic Fields and Radiating System, PHI.
5. A. R. Harish and M. Sachidananda: Antennas and wave propagation, Oxford University Press.
6. K. D. Prasad: Antennas and Wave Propagation, Satya Prakashan.
7. B. L. Smith: Mordern Anteenas, 2nd Edition, Springer, Macmillan India


Dr. SHAILJA SHUKLA
 Jabalpur Engineering College
 Jabalpur - 482 011 (M.P.)

Course Outcomes:

Upon successful completion of course students will be able to:

CO1	Understand various antenna terminologies
CO2	Designing of antenna arrays
CO3	Knowledge of working of various types of antenna
CO4	Synthesize various antenna arrays
CO5	Differentiate between various mechanism of propagation of radio waves

B.E. (CBGS) VI SEMESTER

ELECTRONICS & TELECOMMUNICATION ENGINEERING

MICROPROCESSOR AND MICROCONTROLLERS

Course	Subject Title	Subject Code	Grade for End Sem.		CGPA at the end of every even semester
			T	P	
B.E. (CBGS)	Microprocessor and Microcontroller	EC6002	Min. "D"	Min. "D"	5.0

Unit –I:

Introduction to Microprocessor, Microprocessor 8085 architecture and its operations, The 8085 MPU, Data Transfer operations and instructions, Arithmetic operations and instructions, Logic Operations and instructions, Branch control operations and instructions, Stack and Stack related Operations and instructions, 8085 Interrupts, Writing assembly language programs.

Unit –II:

Intel 8086 Microprocessor: Introduction to 16-bit microprocessors, 8086 pin functions, Minimum and maximum mode operations. 8086 Architecture, register organization, addressing Modes, 8086 Memory banks and Memory organization, 8086 Instruction set and Assembly language programming.

Unit –III:

Advanced microprocessors: Salient features of advanced microprocessors. Review of evolution of advanced microprocessors: 186 / 286 / 386 / 486 / Pentium. Super scalar architecture of Pentium. 80286/386 Memory segmentation with descriptor tables, Privilege levels, Changing privilege levels, Paging including address translation, Page level protection, MMU, cache memory, Virtual memory.

Unit –IV:

INTERFACING: Introduction to the interfacing chips 8255. Interfacing keyboards, printers, LEDs with Intel 8086 Microprocessor. Interfacing of 8254 programmable interval timer, 8259A Programmable interrupt controller & 8257 DMA controller with Intel 8086 Microprocessor. Memory Interfacing: Interfacing of RAM and ROM with Intel 8086 Microprocessor. Serial communication interface: RS 232C standards, Interfacing of USART chip 8251 with Intel 8086 Microprocessor.

Unit –V:

Microcontroller: Introduction to micro controller 8051, its architecture, Register set, operational features, pin description, I/O configuration, interrupts, addressing modes, an overview of 8051 instruction set.

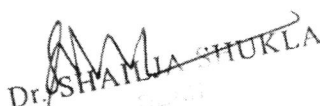
Books Reference :

1. Microprocessor Architecture, Programming and Applications with the 8085 by Ramesh Gaonkar
2. B.B. Brey (PHI), "The Intel Microprocessors, Architecture, Programming and Interfacing".
3. A Triebel & Avtar Singh (PHI), "The 8088 & 8086 Microprocessor".
4. D. Hall (Mc-Graw Hill), "Advanced Microprocessor and Interfacing".
5. Pal (TME), "Microprocessors Principles & Applications".
6. A.P. Mathur (TMA), "Introduction to Microprocessors". Intel Corporation Microprocessors Data manuals.
7. Microprocessor Training Inc., "Microprocessor Fundamentals & Applications (Handson)".

Microprocessor and Microcontrollers Lab

List of Experiments (Expandable):

1. Byte Multiplication.
2. Word Multiplication
3. Packed Bcd From Ascii
4. Bcd Multiplication
5. Bcd Division
6. Bcd Subtraction
7. Signed Byte To Word
8. Scan String For Character
9. If Then Else Implimentation
10. Bcd To Hex (Register Parameter).


Dr. SHANTIA SHUKLA

Jabalpur Engineering College
Jabalpur - 482 011 (M.P.) Microprocessor and Microcontroller

Course Outcomes:

Upon successful completion of course students will be able to:

CO1	Understand the operation of microprocessor 8085
CO2	Knowledge of 8086 microprocessor
CO3	Classify various advance microprocessor
CO4	Interface various devices with microprocessor
CO5	Explain the working of 8051 microcontroller

Microprocessor and Microcontrollers Lab**(Suggested Exercise)****List of Experiments (Expandable):**

1. BYTE MULTIPLICATION.
2. WORD MULTIPLICATION
3. PACKED BCD FROM ASCII
4. BCD MULTIPLICATION
5. BCD DIVISION
6. BCD SUBTRACTION
7. SIGNED BYTE TO WORD
8. SCAN STRING FOR CHARACTER
9. IF THEN ELSE IMPLIMENTATION
10. BCD TO HEX (REGISTER PARAMETER).

B.E. (CBGS) VI SEMESTER

ELECTRONICS & TELECOMMUNICATION ENGINEERING

CMOS VLSI

Course	Subject Title	Subject Code	Grade for End Sem.		CGPA at the end of every even semester
			T	P	
B.E. (CBGS)	CMOS VLSI	EC6003	Min. "D"	Min. "D"	5.0

Unit – I:

Introduction to cmos circuits, circuits & system representation Behavioral representation, structural representation. Physical representation MOS transistor theory. NMOS and PMOS enhancement transistor. Threshold voltage body effect. Mos device design equation. Basic DC equation. Second order effect, MOS models.

Unit - II :

The complementary cmos inverter – DC character, Static load MOS inverters. The differential inverter Tristate inverter. Bipolar devices, diodes, transistors, BICMOS inverters.

Unit - III :

Review of silicon semiconductor technology and basic CMOS technology-n- well and p-well process. Interconnect and circuit Twin-tub process layout design rules and latch-up, latch-up triggering and prevention.

Unit - IV :

Circuit characterization and performance estimation resistance and capacitance estimation, Switching characteristics, CMOS gate transistor sizing, power dissipation. Basic physical design of simple logic gates. CMOS logic structure.

Unit - V :

CMOS design methods. Design strategies. Programmable logic, programmable logic structure, reprogrammable gate arrays. Exiling programmable gate array. Algotonix, concurrent logic, sea of gate and gate array design VHDL as a tool.


Books Reference :

1. Neil, H.E. Wesdte, Kamran Eshraghian, Principles of CMOS VLSI design, Pearson Education.
2. Wyne wolf, Modern VLSI design-system on silicon, Prentics Hall of india
3. Phillip E. Allen and Douglas R holding, CMOS analog Circuit Design, 2nd edition, Oxford University press.

CMOS VLSI LAB

List of Experiments

1. Design of MOS Generator Using any Electronic Design Automation (EDA)- eg. Micro wind / Cadence /Sylva co / Tanner silicon Hipper / Xilinx ISE 9i or any similar software
2. DC MOSFET Curves using EDA.
3. Design of CMOS Logic Gates using EDA.
4. Draw the following CMOS circuits using 0.12 μm and 65 n technology and simulate for transfer characteristics along with 2D and 3D view from 450 angles. Compare power consumption and rise/fall delays in both technologies:
 - a) CMOS Inverter with 0.1pF and 0.1fF capacitance loads, in both cases with equal rise and fall times. Plot output eye diagram also.
 - b) CMOS NAND and NOR gates with 0.01pF load and equal rise and fall times. Comment on area requirement of both gates.
5. To design Current Mirror using CMOS 0.18 micron Technology.
6. Design a basic differential amplifier circuit using current mirror logic. Show gain of amplifier and comment on bandwidth.
7. Design the Schmitt trigger circuit with UTP= 4.5 V and LTP = 2.0 V. Plot transfer curve analysis (with hysteresis effect) VO versus VI.
8. Design a 2-bit parallel adder from schematic and its CMOS layout. List global delay of all nodes. Identify the critical path and comment on its optimization.


DR. SHAILA SHUKLA

Cmos Vlsi

Jabalpur Engineering College
 Jabalpur - 482 011 (M.P.)

Course Outcomes:

Upon successful completion of course students will be able to:

CO1	Understand the working of CMOS
CO2	Characterize CMOS inverter
CO3	Knowledge of CMOS Technology
CO4	Estimation of circuit characteristics of CMOS
CO5	Understand various CMOS design methods.

CMOS VLSI LAB
(Suggested Exercise)

List of Experiments

1. Design of MOS Generator Using any Electronic Design Automation (EDA)- eg. Microwind / Cadence /Sylvaco / Tanner silicon HiPer / Xilinx ISE 9i or any similar software
2. DC MOSFET Curves using EDA.
3. Design of CMOS Logic Gates using EDA.
4. Draw the following CMOS circuits using 0.12 μm and 65 ntechnology and simulate for transfer characteristics along with 2D and 3D view from 450 angles. Compare power consumption and rise/fall delays in both technologies:
 - a. CMOS Inverter with 0.1pF and 0.1fF capacitance loads, in both cases with equal rise and fall times. Plot output eye diagram also.
 - b. CMOS NAND and NOR gates with 0.01pF load and equal rise and fall times. Comment on area requirement of both gates.
5. To design Current Mirror using CMOS 0.18 micron Technology.
6. Design a basic differential amplifier circuit using current mirror logic. Show gain of amplifier and comment on bandwidth.
7. Design the Schmitt trigger circuit with $UTP = 4.5\text{ V}$ and $LTP = 2.0\text{ V}$. Plot transfer curve analysis (with hysteresis effect) V_O versus V_I .
8. Design a 2-bit parallel adder from schematic and its CMOS layout. List global delay of all nodes. Identify the critical path and comment on its optimization.

B.E. (CBGS) VI SEMESTER

ELECTRONICS & TELECOMMUNICATION ENGINEERING

DIGITAL SIGNAL PROCESSING

Course	Subject Title	Subject Code	Grade for End Sem.		CGPA at the end of every even semester
			T	P	
B.E. (CBGS)	Digital Signal Processing	EC6004	Min. "D"	Min. "D"	5.0

Unit – I:

Discrete-Time Signals and Systems : Review of Discrete-Time Sequences and Systems, Linear constant coefficient difference equations, Derivation of transfer function of LTI systems, Frequency Domain Representation of discrete time signals & systems, Signal flow Graph representation of digital network, matrix representation, introduction to Two dimensional sequences and systems.

Unit – II:

The Z-Transform Applications: The review of Direct Z-transform and Inverse- Z transform ,Mapping of S-domain to Z- domain, System Stability in Z-domain, Rational Z-transforms, chirp – Z transform, Two dimensional Z-transform. Design of LTI systems using Z-transform.

Unit – III:

Frequency Analysis of Discrete Time Signals: Discrete Fourier series (DFS), Comparison of the DFS and Discrete Fourier Transform (DFT), Properties of DFT , Circular Convolution , Two dimensional DFT ,FFT algorithms, Radix-2 FFT Algorithm, Goertzel's Algorithm, Decimation in time, Decimation in frequency algorithm, Decomposition for 'N' composite number.

Unit – IV:

Basic filter structures : Recursive and non -recursive networks, System connectivity, Basic structures of IIR and FIR filters, Determining of system response, Impulse response and transfer function of filters, Determining impulse response using Recursion formula ,finite word -length effects in digital filters.

Unit – V:

Digital filters Design Techniques: Design of IIR and FIR digital filters, Impulse invariant and bilinear transformation, windowing techniques- rectangular and other windows, Application of MATLAB for design of digital filters, Concept of Adaptive filtering and applications.

Books Reference:

1. A.V. Oppenheim and R. W. Schaffer: Digital Signal Processing, Prentice Hall.
2. L.R. Rabiner and B. Gold: Theory and Application of Digital Signal Processing, Prentice Hall
3. John. G. Proakis and Monolakis: Digital Signal Processing, Pearson Education
4. Salivahanan and Vallavraj: Digital Signal Processing, Mc Graw Hill.
5. S. K. Mitra: Digital Signal Processing- A Computer based Approach, Mc Graw Hill.
6. Schilling and Harris: Fundamentals of DSP using MATLAB, Cengage Learning.

DIGITAL SIGNAL PROCESSING LAB

List of Experiments:

The following practical should be performed using Mat lab/ any DSP software –

1. Generation, analysis and plots of discrete-time signals.
2. Implementation of operations on sequences (addition, multiplication, scaling, shifting, folding etc).
3. Implementation of Linear time-invariant (LTI) systems and testing them for stability and causality.
4. Computation and plots of z-transforms, verification of properties of z-transforms.
5. Computation and plot of DFT of sequences, verification of properties of DFT.
6. Computation and plots of linear/circular convolution of two sequences.
7. Computation of radix-2 FFT- Decimation in time and Decimation in frequency.
8. Implementation of IIR and FIR filter structures (direct, cascade, parallel etc).
9. Design of windowing techniques of FIR Filter.


Dr. SHAILJA SHUKLA

Jabalpur Engineering College
Jabalpur - 482 011 (M.P.)

CO1	Represent signal and system in various domain
CO2	Design of LTI system using Z Transform
CO3	Analyze the frequency if Discrete Time Signal
CO4	Classify various Filter structures
CO5	Designing of various Digital Filters

DIGITAL SIGNAL PROCESSING LAB

(Suggested Exercise)

List of experiments:

The following practical should be performed using Matlab/ any DSP software –

1. Generation, analysis and plots of discrete-time signals.
2. Implementation of operations on sequences (addition, multiplication, scaling, shifting, folding etc).
3. Implementation of Linear time-invariant (LTI) systems and testing them for stability and causality.
4. Computation and plots of z-transforms, verification of properties of z-transforms.
5. Computation and plot of DFT of sequences, verification of properties of DFT.
6. Computation and plots of linear/circular convolution of two sequences.
7. Computation of radix-2 FFT- Decimation in time and Decimation in frequency.
8. Implementation of IIR and FIR filter structures (direct, cascade, parallel etc).
9. Design of windowing techniques of FIR Filter.

B.E. (CBGS) VI SEMESTER

ELECTRONICS & TELECOMMUNICATION ENGINEERING

(ELECTIVE - II) IPR (INTELLECTUAL PROPERTY RIGHT)

Course	Subject Title	Subject Code	Grade for End Sem.		CGPA at the end of every even semester
			T	P	
B.E. (CBGS)	(Elective - II) IPR (Intellectual Property Right)	EC6005A	Min. "D"	Min. "D"	5.0

Unit -I:

General overview of intellectual property, introduction to intellectual property, the concept of intellectual property, different categories of IP instruments, Rational behind intellectual property, Rights of the owner of the intellectual property, other individual and the society-striking balance, Enforcement of intellectual property rights. Intellectual property and the constitution of India.

Unit -II:

Emerging issues in intellectual property, introduction advances in information and communication technology challenges for intellectual property in digital economy, Electronic commerce, Internet domain names disputes, Biotechnology and intellectual property. Human Genome, Traditional Knowledge, Folk lore Biodiversity and intellectual property Biodiversity.

Unit -III:

Intellectual property rights – Indian Scenario :- Introduction to the intellectual property in Indian scenario, History of intellectual property Legislation, Overview of intellectual property Law in India, The Indian Patent Law, intellectual property acts enacted by India major International treaties signed by India.

Unit -IV:

Role of patents in promoting Invention, Innovation and technology and technology development. Introduction instruments of Rights and privileges. Patent application procedures, Patent and technology development

Unit -V:

Dichotomy between Industrial property and copyright and Related rights Introduction copyright Vs intellectual property

Books Reference :

1. Intellectual property Wright by Neeraj Pandey
2. Intellectual property Wright by C. V. Raju
3. Intellectual property Wright by M. Ashok Kumar



Dr. SHAILJA SHUKLA

Jabalpur Engineering College
Jabalpur - 482 011 (M.P.)

B.E. (CBGS) VI SEMESTER

ELECTRONICS & TELECOMMUNICATION ENGINEERING

(ELECTIVE - II) DATA COMMUNICATION & COMPUTER NETWORK

Course	Subject Title	Subject Code	Grade for End Sem.		CGPA at the end of every even semester
			T	P	
B.E. (CBGS)	(Elective - II) Data Communication & Computer Network	EC6005B	Min. "D"	Min. "D"	5.0

Unit -I:

Introduction to Data Communication and Networks:

Data Communication, Networks – Physical structures; different topologies, Categories of Networks: LAN, MAN, WAN, Interconnection of networks, The Internet, Protocols and Standards, Standards Organizations. Network Models, Layered tasks, The OSI model, different layers in OSI model. TCP/IP protocol suite ; different layers, addressing, - physical, logical, port and specific addresses; Session, Presentation and Application layers, working in internet.

Unit – II:

Physical Layer :

Digital-to-Digital Conversion-Line Coding, Line Coding Scheme, Block Coding, Scrambling, Multiplexing – Frequency Division, Wavelength Division, Synchronous Time Division, Statistical Time Division Multiplexing. Structure of Circuit and Packet switches, Dial-up Modems, Digital Subscriber Line - ADSL, ADSL Lite, HDSL, SDSL, VDSL, Cable TV for Data Transfer- Bandwidth, Sharing, Physical Layer. Bluetooth- Architecture, Radio Layer, Baseband Layer, L2CAP.

Unit – III:

Data Link Layer:

Block Coding - Error Detection, Error Correction, Hamming Distance, Minimum Hamming Distance. Linear Block Codes, Cyclic Codes - Cyclic Redundancy Check, Cyclic Code Analysis, Advantages. Checksum, Framing - Fixed and Variable-Size. Flow and Error Control, Protocols, Noiseless Channels – Simplest and Stop-and-Wait Protocols. Noisy Channels - Stop-and-Wait Automatic Repeat Request, Go-Back-N Automatic Repeat Request, Selective reject.

Unit - IV:

Medium Access:

Random Access- ALOHA, Carrier Sense Multiple Access (CSMA), Carrier Sense Multiple Access with Collision Detection (CSMA/CD), Carrier Sense Multiple Access with Collision Avoidance (CSMA/CA). Controlled Access-Reservation, Polling, Token Passing. Channelization- Frequency-Division Multiple Access (FDMA), Time-Division Multiple Access (TDMA), Code-Division Multiple Access (CDMA). IEEE Standards, Standard Ethernet, Fast Ethernet, Gigabit Ethernet, IEEE 802.11- Architecture, MAC Sub layer, Addressing Mechanism.

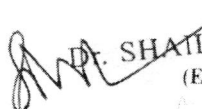
Unit V:

Connecting LANs and WAN:

Connecting Devices- Passive Hubs, Repeaters, Active Hubs, Bridges, Two-Layer Switches, Three-Layer Switches, Gateway. Backbone Networks-Bus, Star, Connecting Remote LANs. Virtual LANs -Membership, Configuration, Communication betweenSwitches. Network layer – logical addressing - .IPv4Addresses- Address Space, Notation, Classful Addressing, Classless Addressing, Network Address Translation (NAT). IPv6 Addresses - Structure and AddressSpace. Internetworking -Need for Network Layer, Internet as a Datagram Network, Internet as a Connectionless Network. IPv4- Datagram, Fragmentation, Checksum, Options. IPv6 - Advantages, Packet Format, Extension Headers. Transition from IPv4 to IPv6. Address Mapping- Logical to Physical Address, Physical to Logical Address.

Books Reference:

1. B. A. Forouzan and Sophia Chung Fegan: Data Communications and Networking, 4th Ed, TMH.
2. W. Tomasi: Introduction to Data Communications and Networking, Pearson Education.
3. A. S. Tanenbaum: Computer Networks, Pearson Education.
4. W. Stalling: Data and Computer Communication, Pearson Education.
5. P. C. Gupta: Data Communications and Computer Networks, PHI.
6. A. Elahi and M. Elahi: Data Network and Internet-Communications Technology, Cengage Learning.
7. Duck: Data Communication and Networking, Pearson Education

 **SHAILJA SHUKLA**

(Elective - II) Data Communication & Computer Network

Jabalpur Engineering College
Jabalpur - 482 011 (M.P.)

References:

1. B. A. Forouzan and Sophia Chung Fegan: Data Communications and Networking, 4th Ed, TMH.
2. W. Tomasi: Introduction to Data Communications and Networking, Pearson Education.
3. A. S. Tanenbaum: Computer Networks, Pearson Education.
4. W. Stalling: Data and Computer Communication, Pearson Education.
5. P. C. Gupta: Data Communications and Computer Networks, PHI.
6. A. Elahi and M. Elahi: Data Network and Internet-Communications Technology, Cengage Learning.
7. Duck: Data Communication and Networking, Pearson Education

Course Outcomes:

Upon successful completion of course students will be able to:

CO1	Classify various type of Data Communication Network
CO2	Understand design constraints of physical layer
CO3	Analyze various error detection and correction technologies
CO4	Understand various addressing mechanism
CO5	Understand various types of connecting devices

B.E. (CBGS) VI SEMESTER

ELECTRONICS & TELECOMMUNICATION ENGINEERING

(ELECTIVE - II) POWER ELECTRONICS

Course	Subject Title	Subject Code	Grade for End Sem.		CGPA at the end of every even semester
			T	P	
B.E. (CBGS)	(Elective - II) Power Electronics	EC6005C	Min. "D"	Min. "D"	5.0

Unit-I:

Power Supplies:

Power supply, rectifiers (half wave, full wave), performance parameters of power supplies, filters (capacitor, inductor, inductor-capacitor, pi filter), bleeder resistor, voltage multipliers. Regulated power supplies (series and shunt voltage regulators, fixed and adjustable voltage regulators, current regulator), switched regulator (SMPS), comparison of linear and switched power supply, switch mode converter (flyback, buck, boost, buk-boost, cuk converters)

Unit-II:

Thrusters:

Silicon controlled rectifies (SCR), constructional features, principle of operation, SCR terminology, turn-on methods, turn-off methods, triggering methods of SCR circuits, types of commutation, comparison of thyristors and transistors, thermal characteristics of SCR, causes of damage to SCR, SCR overvoltage protection circuit, series and parallel operation of SCRs, Line commutated converters (half wave rectifier with inductive and resistive load, single phase and three phase full wave rectifiers).

Unit-III:

Other members of SCR family :

Triacs, Diacs, Quadacs, recovery characteristics, fast recovery diodes, power diodes, power transistor, power MOSFET, Insulated gate bipolar transistor (IGBT), loss of power in semiconductor devices, comparison between power MOSFET, power transistor and power IGBT.

Unit-IV:

Applications of OP-AMP :

Basics of OP-AMP, relaxation oscillator, window comparator, Op-comp as rectangular to triangular pulse Converter and vice-versa, Wien bridge oscillator, function generator, frequency response of OP-AMP, Simplified circuit diagram of OP-AMP, power supplies using OP-AMP, filters (low-pass, high pass) using OP-AMP.

Unit-V:

Programmable Logic Controller (PLC) :

Functions, applications, advantages and disadvantages of PLC over conventional relay controllers, Comparison of PLC with process control computer system, factors to be considered in selecting PLC, functional block diagram of PLC, microprocessor in PLC, memory, input and output modules (interface cards), sequence of operations in a PLC, status of PLC, event driven device, ladder logic language, simple process control applications of PLC, Programming examples.

Books Reference:

1. Bishwanath Paul: Industrial Electronics and control, PHI Learning.
2. Rashid: Power Electronics- Circuits, devices and applications, Pearson Education.
3. Singh and Khanchandani: Power Electronics, TMH
4. Bhimbra: Power Electronics, Khanna Publishers.
5. Moorthi: Power Electronics, Oxford University Press.
6. Webb: Programmable Logic Controllers- Principles and Applications, PHI Learning.
7. Petruzulla: Programmable Logic Controllers, TMH.


DR. SHAILJA SHUKLA

Jabalpur Engineering College
Jabalpur - 482 011 (M.P.)

B.E. (CBGS) VI SEMESTER

ELECTRONICS & TELECOMMUNICATION ENGINEERING

(ELECTIVE - II) OPERATING SYSTEM

Course	Subject Title	Subject Code	Grade for End Sem.		CGPA at the end of every even semester
			T	P	
B.E. (CBGS)	(Elective - II) Operating System	EC6005D	Min. "D"	Min. "D"	5.0

Unit-I:

Operating Systems Overview: Computer System Overview-Basic Elements, Instruction Execution, Interrupts, Memory Hierarchy, Cache Memory, Direct Memory Access, Multiprocessor and Multicore Organization. Operating system overview-objectives and functions, Evolution of Operating System.- Computer System Organization- Operating System Structure and Operations- System Calls, System Programs, OS Generation and System Boot.

Unit -II:

Process Management: Processes-Process Concept, Process Scheduling, Operations on Processes, Interprocess Communication; Threads- Overview, Multicore Programming, Multithreading Models; Windows 7 - Thread and SMP Management. Process Synchronization - Critical Section Problem, Mutex Locks, Semaphores, Monitors CPU Scheduling and Deadlocks.

Unit -III :

Storage Management :Main Memory-Contiguous Memory Allocation, Segmentation, Paging, 32 and 64 bit architecture Examples; Virtual Memory- Demand Paging, Page Replacement, Allocation, Thrashing , Allocating Kernel Memory, OS Examples.

Unit -IV:

I/O Systems: Mass Storage Structure- Overview, Disk Scheduling and Management; File System Storage- File Concepts, Directory and Disk Structure, Sharing and Protection; File System Implementation- File System Structure, Directory Structure, Allocation Methods, Free Space Management, I/O Systems.

Unit V:

Case Study: Linux System- Basic Concepts , System Administration-Requirements for Linux System Administrator, Setting up a LINUX Multifunction Server, Domain Name System, Setting Up Local Network Services; Virtualization- Basic Concepts, Setting Up Xen, VMware on Linux Host and Adding Guest OS.

Books Reference :

1. Tanenbaum A, "Modern Operating Systems", PHI 2nd Ed
2. Silberchatz & Galvin, "Operating System Concepts", Addison Wesley.


DR. SHAILJA SHUKLA


Jabalpur Engineering College
Jabalpur - 482 011 (M.P.)

B.E. (CBGS) VI SEMESTER
ELECTRONICS & TELECOMMUNICATION ENGINEERING
DEPARTMENTAL LAB-III (DEPARTMENTAL CHOICE)
VHDL/VERILOG

Course	Subject Title	Subject Code	Grade for End Sem.		CGPA at the end of every even semester
			T	P	
B.E. (CBGS)	Departmental Lab-III Departmental Choice) VHDL/Verilog	EC6006	Min. "D"	Min. "D"	5.0

List of Experiments:

1. Design of all logic gates using VHDL.
2. Develop a VHDL code for full adder using structural style of modeling.
3. Develop a VHDL code for Half adder using data flow style of modeling.
4. Develop a VHDL code for 4x1 multiplexer using data flow style of modeling.
5. Develop a VHDL code for 3x8 decoder using data flow style of modeling.
6. Develop a VHDL code for D – Flip Flop.
7. Develop a VHDL code for S-R – Flip Flop.
8. Develop a VHDL code for Binary to Gray converter.
9. Develop a VHDL code for Up counter.
10. Develop a VHDL code for Down counter.


Dr. SHAILJA SHUKLA
 Assistant Professor
 Jabalpur Engineering College
 Jabalpur - 482 011 (M.P.)